providing the amorphous semiconductor film with an element which promotes crystallization of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film by a first heat treatment to form a crystalline semiconductor film;

introducing an impurity element belonging to Group 15 into a first portion of the crystalline semiconductor film while a second portion of the crystalline semiconductor film is not provided with the impurity element;

D1 cont

wherein the first and second portions of the crystalline semiconductor film are in contact with the insulating surface over the substrate;

performing a second heat treatment so that the element contained in the second portion is moved to the first portion in a direction parallel to the insulating surface; and

patterning the crystallized semiconductor film to form a crystalline semiconductor island in the second portion thereby removing the first portion of the crystalline semiconductor film;

forming an active layer of the thin film transistor using the crystalline semiconductor island,

wherein the second heat treatment is performed in a temperature range not exceeding a glass transition point of the substrate.

3. (Amended) A method according to claim 1, wherein the second heat treatment is performed in the temperature range from 500 to 700°C.

5. (Amended) A method according to claim 1, wherein the second heat treatment is furnace annealing.

9. (Amended) A method of manufacturing a semiconductor device including at least a thin film transistor, said method comprising the steps of:

forming an amorphous semiconductor film comprising silicon over a substrate having an insulating surface;

selectively providing a first portion of the amorphous semiconductor film with an element which promotes crystallization of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film by a first heat treatment to form a crystalline semiconductor film, so that a crystallization proceeds from the first portion in a lateral direction to the insulating surface;

introducing an impurity element belonging to Group 15 into a second portion of the crystalline semiconductor film while a third portion of the crystalline semiconductor film is not provided with the impurity element;

wherein the second and third portions of the crystalline semiconductor film are in contact with the insulating surface over the substrate;

performing a second heat treatment so that the element contained in the third portion is moved to the second portion in a lateral direction to the insulating surface; and

patterning the crystalline semiconductor film to form a crystalline semiconductor island in the third portion thereby removing the second portion of the crystalline semiconductor film;

forming an active layer of the thin film transistor using the crystalline semiconductor island,

wherein the second heat treatment is performed in a temperature range not exceeding a glass transition point of the substrate.

11. (Amended) A method according to claim 9, wherein the second heat treatment is performed in the temperature range from 500 to 700°C.

13. (Amended) A method according to claim 9, wherein the second heat treatment is furnace annealing.

17. (Amended) A method of manufacturing a semiconductor device including at least a thin film transistor, said method comprising the steps of:

forming an amorphous semiconductor film comprising silicon over a substrate having an insulating surface;

providing the amorphous semiconductor film with an element which promotes crystallization of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film by a first heat treatment to form a crystalline semiconductor film;

irradiating a laser light or an intense light to the crystalline semiconductor film;

introducing an impurity element belonging to Group 15 into a first portion of the crystalline semiconductor film after the irradiating step, while a second portion of the crystalline semiconductor film is not provided with the impurity element;

wherein the first and second portions of the crystalline semiconductor film are in contact with the insulating surface over the substrate;

performing a second heat treatment so that the element contained in the second portion is moved to the first portion in a lateral direction to the insulating surface;

patterning the crystalline semiconductor film to form a crystalline semiconductor island in the second portion thereby removing the second portion of the crystalline semiconductor film;

forming an active layer of the thin film transistor using the crystalline semiconductor island,

wherein the second heat treatment is performed in a temperature range not exceeding a glass transition point of the substrate.

19. (Amended) A method according to claim 17, wherein the second heat treatment is performed in the temperature range from 500 to 700°C.

21. (Amended) A method according to claim 17, wherein the second heat treatment is furnace annealing.

25. (Amended) A method of manufacturing a semiconductor device including at least a thin film transistor, said method comprising the steps of:

forming an amorphous semiconductor film comprising silicon over a substrate having an insulating surface;

selectively providing a first portion of the amorphous semiconductor film with an element which promotes crystallization of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film by a first heat treatment to form a crystalline semiconductor film, so that a crystallization proceeds from the first portion of the amorphous semiconductor film in a lateral direction to the insulating surface;

Dio cont

irradiating a laser light or an intense light to the crystalline semiconductor film;

introducing an impurity element belonging to Group 15 into a second portion of the crystalline semiconductor film after the irradiating step, while a third portion of the crystalline semiconductor film is not introduced with the impurity element;

wherein the second and third portions of the crystalline semiconductor film are in contact with the insulating surface over the substrate;

performing a second heat treatment so that the element contained in the third portion is moved to the second portion in a lateral direction to the insulating surface;

patterning the crystalline semiconductor film to form a crystalline semiconductor island in the third portion thereby removing the second portion of the crystalline semiconductor film;

D10 end

forming an active layer of the thin film transistor using the crystalline semiconductor island,

wherein the second heat treatment is performed in the temperature range not exceeding a glass transition point of the substrate.

D11 27. (Amended) A method according to claim 25, wherein the second heat treatment is performed in the temperature range from 500 to 700°C.

D12 29. (Amended) A method according to claim 25, wherein the second heat treatment is furnace annealing.

D13 33. (Amended) A method according to claim 1, wherein said step of introducing the impurity element belonging to Group 15 is performed by plasma doping.

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36. (Amended) A method according to claim 9, wherein said step of introducing the impurity element belonging to Group 15 is performed by plasma doping.

39. (Amended) A method according to claim 17, wherein said step of introducing the impurity element belonging to Group 15 is performed by plasma doping.

42. (Amended) A method according to claim 25, wherein said step of introducing the impurity element belonging to Group 15 is performed by plasma doping.

45. (Amended) A method of manufacturing a semiconductor device including at least a thin film transistor, said method comprising the steps of:

forming an amorphous semiconductor film comprising silicon over a substrate having an insulating surface;

providing the amorphous semiconductor film with an element which promotes crystallization of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film by a first heat treatment to form a crystalline semiconductor film;

introducing an impurity element belonging to Group 15 into a first portion of the crystalline semiconductor film while a second portion of the crystalline semiconductor film is not provided with the impurity element;

wherein the first and second portions of the crystalline semiconductor film are in contact with the insulating surface over the substrate;

performing a second heat treatment so that the element contained in the second portion is moved to the first portion in a lateral direction to the insulating surface;

D17 cont

patterning the crystalline semiconductor film to form a crystalline semiconductor island in the second portion thereby removing the first portion of the crystalline semiconductor film;

forming a gate insulating film over the crystalline semiconductor island;

forming at least one gate electrode comprising a metal on the gate insulating film;

doping an impurity element into at least a second portion of the crystalline semiconductor island to form a lightly doped drain region; and

forming at least a source region and a drain region by doping an impurity element into third portions of the crystalline semiconductor island,

wherein the second heat treatment is performed in a temperature range not exceeding a glass transition point of the substrate.

46. (Amended) A method according to claim 45, wherein the second heat treatment is performed in the temperature range from 500 to 700°C.

49. (Amended) A method according to claim 45, wherein said step of introducing the impurity element belonging to Group 15 is performed by plasma doping.

52. (Amended) A method of manufacturing a semiconductor device including at least a thin film transistor, said method comprising the steps of:

forming an amorphous semiconductor film comprising silicon over a substrate having an insulating surface;

providing the amorphous semiconductor film with an element which promotes crystallization of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film by a first heat treatment to form a crystalline semiconductor film;

introducing an impurity element belonging to Group 15 into a first portion of the crystalline semiconductor film while a second portion of the crystalline semiconductor film is not provided with the impurity element;

performing a second heat treatment so that the element contained in the second portion is moved to the first portion in a lateral direction to the insulating surface;

D30 cont

patterning the crystalline semiconductor film to form a crystalline semiconductor island in the second portion thereby removing the first portion of the crystalline semiconductor film;

forming a gate insulating film over the crystalline semiconductor island;

forming at least one gate electrode comprising a metal on the gate insulating film;

doping an impurity element into at least a second portion of the crystalline semiconductor island to form a lightly doped drain region;

forming at least a source region and a drain region by doping an impurity element into third portions of the crystalline semiconductor island;

forming an interlayer insulating film comprising silicon over the gate electrode;

forming an interlayer insulating film comprising an organic resin film over the interlayer insulating film; and

forming a pixel electrode that is electrically connected to the source region or drain region through a contact hole over the interlayer film;

wherein the second heat treatment is performed in a temperature range not exceeding a glass transition point of the substrate.

D20 end

53. (Amended) A method according to claim 52, wherein the second heat treatment is performed in the temperature range from 500 to 700°C.

D21

57. (Amended) A method according to claim 52, wherein said step of introducing the impurity element belonging to Group 15 is performed by plasma doping.

D22

76. (Amended) A method according to claim 1, wherein the element in the crystalline semiconductor island after the second heat treatment has a concentration in a range of 1×10^{18} atoms/cm^3 or lower.

D23

77. (Amended) A method according to claim 9, wherein the element in the crystalline semiconductor island after the second heat treatment has a concentration in a range of 1×10^{18} atoms/cm^3 or lower.

78. (Amended) A method according to claim 17, wherein the element in the crystalline semiconductor island after the second heat treatment has a concentration in a range of 1×10^{18} atoms/cm^3 or lower.

D23 cont

79. (Amended) A method according to claim 25, wherein the element in the crystalline semiconductor island after the second heat treatment has a concentration in a range of 1×10^{18} atoms/cm^3 or lower.

80. (Amended) A method according to claim 45, wherein the element in the crystalline semiconductor island after the second heat treatment has a concentration in a range of 1×10^{18} atoms/cm^3 or lower.

81. (Amended) A method according to claim 52, wherein the element in the crystalline semiconductor island after the second

heat treatment has a concentration in a range of 1×10^{18} atoms/cm^3 or lower.

Please add claims 82-115.

-- 82. (New) A method of manufacturing a semiconductor device including at least a thin film transistor, said method comprising the steps of:

forming an amorphous semiconductor film on an insulating surface;

providing the amorphous semiconductor film with an element which promotes crystallization of the amorphous semiconductor film;

performing a first heat treatment to crystallize the amorphous semiconductor film;

introducing an impurity element belonging to Group 15 into a first portion of the crystalline semiconductor film while a second portion of the crystalline semiconductor film is not provided with the impurity element;

wherein the first and second portions of the crystalline semiconductor film are in contact with the insulating surface over the substrate;

performing a second heat treatment so that the element contained in the second portion is moved to the first portion in a direction parallel to the insulating surface;

patterning the crystallized semiconductor film to form a crystalline semiconductor island in the second portion thereby removing the first portion of the crystalline semiconductor film; and

forming an active layer of the thin film transistor using the crystalline semiconductor island.

Dup cont

83. (New) A method according to claim 82, wherein the crystalline semiconductor film has grain boundaries.

84. (New) A method according to claim 82, wherein the second heat treatment is performed in the temperature range from 500 to 700°C.

85. (New) A method according to claim 82, wherein the second heat treatment is furnace annealing.

86. (New) A method according to claim 82, wherein the element which promotes crystallization is at least one element

selected from the group of elements consisting of Ni, Co, Fe, Pd, Pt, Cu and Au.

87. (New) A method according to claim 82, wherein the impurity element belonging to Group 15 is at least one element selected from the group of elements consisting of P, N, As, Sb, and Bi.

88. (New) A method of manufacturing a semiconductor device including at least a thin film transistor, said method comprising the steps of:

forming an amorphous semiconductor film on an insulating surface;

providing the amorphous semiconductor film with an element which promotes crystallization of the amorphous semiconductor film;

performing a first heat treatment to crystallize the amorphous semiconductor;

irradiating a laser light or an intense light to the crystalline semiconductor film;

introducing an impurity element belonging to Group 15 into a first portion of the crystalline semiconductor film after

the irradiating step, while a second portion of the crystalline semiconductor film is not provided with the impurity element;

wherein the first and second portions of the crystalline semiconductor film are in contact with the insulating surface over the substrate;

performing a second heat treatment so that the element contained in the second portion is moved to the first portion in a lateral direction to the insulating surface;

patterning the crystalline semiconductor film to form a crystalline semiconductor island in the second portion thereby removing the second portion of the crystalline semiconductor film; and

forming an active layer of the thin film transistor using the crystalline semiconductor island.

89. (New) A method according to claim 88, wherein the crystalline semiconductor film has grain boundaries.

90. (New) A method according to claim 88, wherein the second heat treatment is performed in the temperature range from 500 to 700°C.

91. (New) A method according to claim 88, wherein the second heat treatment is furnace annealing.

92. (New) A method according to claim 88, wherein the element which promotes crystallization is at least one element selected from the group of elements consisting of Ni, Co, Fe, Pd, Pt, Cu and Au.

D24 cont

93. (New) A method according to claim 88, wherein the impurity element belonging to Group 15 is at least one element selected from the group of elements consisting of P, N, As, Sb, and Bi.

Sub E9

94. (New) A method of manufacturing a semiconductor device including at least a thin film transistor, said method comprising the steps of:

forming an amorphous semiconductor film on an insulating surface;

providing the amorphous semiconductor film with an element which promotes crystallization of the amorphous semiconductor film;

performing a first heat treatment to crystallize the amorphous semiconductor film;

introducing an impurity element belonging to Group 15 into a first portion of the crystalline semiconductor film while a second portion of the crystalline semiconductor film is not provided with the impurity element;

wherein the first and second portions of the crystalline semiconductor film are in contact with the insulating surface over the substrate;

performing a second heat treatment so that the element contained in the second portion is moved to the first portion in a direction parallel to the insulating surface;

forming a crystalline semiconductor island by removing the first portion and a part of the second portion; and

forming an active layer of the thin film transistor using the crystalline semiconductor island.

95. (New) A method according to claim 94, wherein the crystalline semiconductor film has grain boundaries.

96. (New) A method according to claim 94, wherein the second heat treatment is performed in the temperature range from 500 to 700°C.

97. (New) A method according to claim 94, wherein the second heat treatment is furnace annealing.

98. (New) A method according to claim 94, wherein the element which promotes crystallization is at least one element selected from the group of elements consisting of Ni, Co, Fe, Pd, Pt, Cu and Au.

D24 last

99. (New) A method according to claim 94, wherein the impurity element belonging to Group 15 is at least one element selected from the group of elements consisting of P, N, As, Sb, and Bi.

5b2c10 100. (New) A method of manufacturing a semiconductor device including at least a thin film transistor, said method comprising the steps of:

forming an amorphous semiconductor film on an insulating surface;

providing the amorphous semiconductor film with an element which promotes crystallization of the amorphous semiconductor film;

performing a first heat treatment to crystallize the amorphous semiconductor;

irradiating a laser light or an intense light to the crystalline semiconductor film;

introducing an impurity element belonging to Group 15 into a first portion of the crystalline semiconductor film after the irradiating step, while a second portion of the crystalline semiconductor film is not provided with the impurity element;

wherein the first and second portions of the crystalline semiconductor film are in contact with the insulating surface over the substrate;

performing a second heat treatment so that the element contained in the second portion is moved to the first portion in a lateral direction to the insulating surface;

forming a crystalline semiconductor island by removing the first portion and a part of the second portion; and

forming an active layer of the thin film transistor using the crystalline semiconductor island.

101. (New) A method according to claim 100, wherein the crystalline semiconductor film has grain boundaries.

102. (New) A method according to claim 100, wherein the second heat treatment is performed in the temperature range from 500 to 700°C.

103. (New) A method according to claim 100, wherein the second heat treatment is furnace annealing.

104. (New) A method according to claim 100, wherein the element which promotes crystallization is at least one element selected from the group of elements consisting of Ni, Co, Fe, Pd, Pt, Cu and Au.

105. (New) A method according to claim 100, wherein the impurity element belonging to Group 15 is at least one element selected from the group of elements consisting of P, N, As, Sb, and Bi.

106. (New) A method according to claim 1, wherein the element which promotes crystallization is provided with the amorphous semiconductor layer by introducing into the amorphous semiconductor film or applying a layer containing the element to the amorphous semiconductor film.

107. (New) A method according to claim 9, wherein the element which promotes crystallization is provided with the amorphous semiconductor layer by introducing into the amorphous

semiconductor film or applying a layer containing the element to the amorphous semiconductor film.

108. (New) A method according to claim 17, wherein the element which promotes crystallization is provided with the amorphous semiconductor layer by introducing into the amorphous semiconductor film or applying a layer containing the element to the amorphous semiconductor film.

D24 cont

109. (New) A method according to claim 25, wherein the element which promotes crystallization is provided with the amorphous semiconductor layer by introducing into the amorphous semiconductor film or applying a layer containing the element to the amorphous semiconductor film.

110. (New) A method according to claim 45, wherein the element which promotes crystallization is provided with the amorphous semiconductor layer by introducing into the amorphous semiconductor film or applying a layer containing the element to the amorphous semiconductor film.

111. (New) A method according to claim 52, wherein the element which promotes crystallization is provided with the

amorphous semiconductor layer by introducing into the amorphous semiconductor film or applying a layer containing the element to the amorphous semiconductor film.

112. (New) A method according to claim 82, wherein the element which promotes crystallization is provided with the amorphous semiconductor layer by introducing into the amorphous semiconductor film or applying a layer containing the element to the amorphous semiconductor film.

D34 cont

113. (New) A method according to claim 88, wherein the element which promotes crystallization is provided with the amorphous semiconductor layer by introducing into the amorphous semiconductor film or applying a layer containing the element to the amorphous semiconductor film.

114. (New) A method according to claim 94, wherein the element which promotes crystallization is provided with the amorphous semiconductor layer by introducing into the amorphous semiconductor film or applying a layer containing the element to the amorphous semiconductor film.

115. (New) A method according to claim 100, wherein the element which promotes crystallization is provided with the amorphous semiconductor layer by introducing into the amorphous semiconductor film or applying a layer containing the element to the amorphous semiconductor film. --